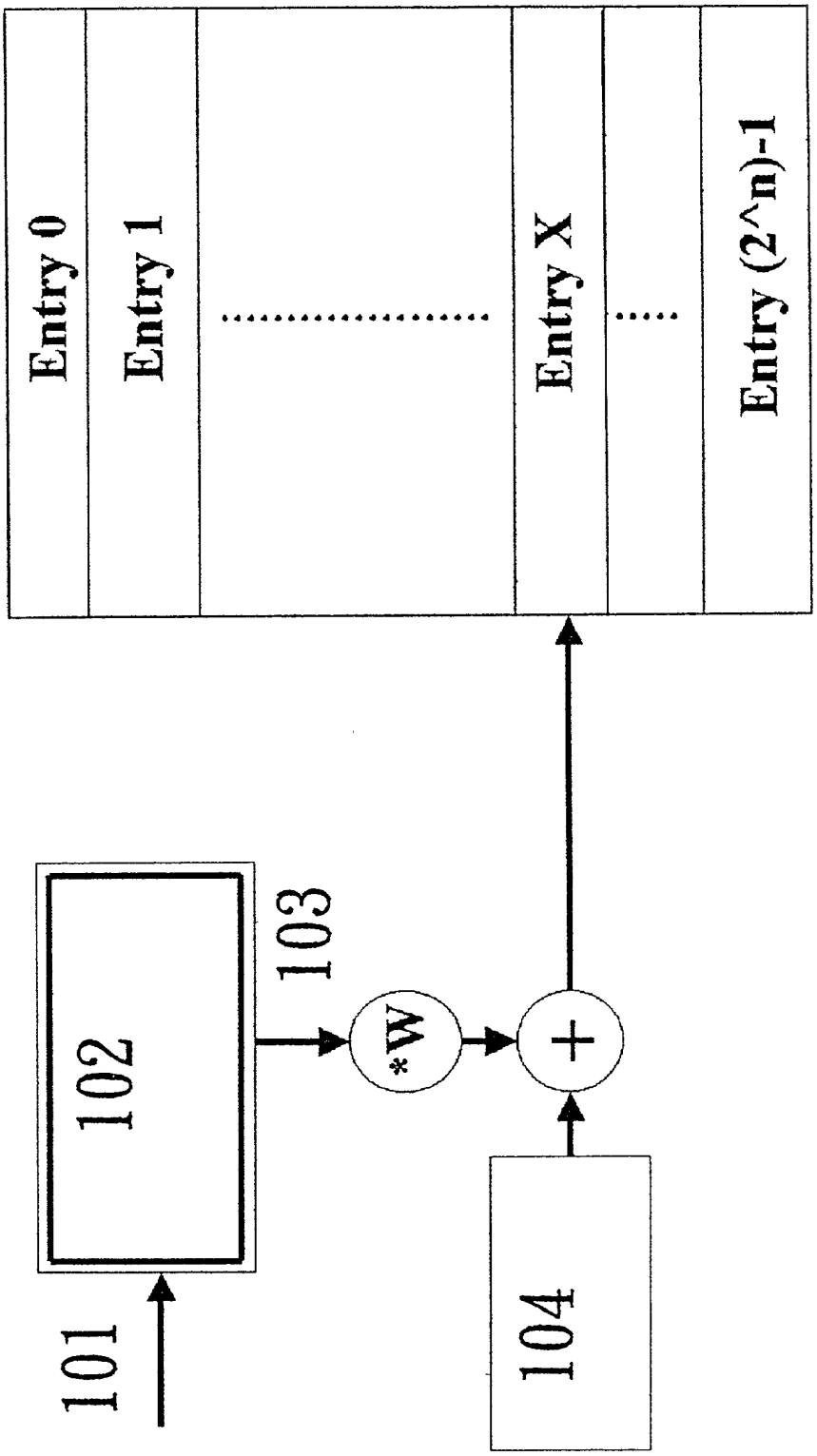

FIG 1

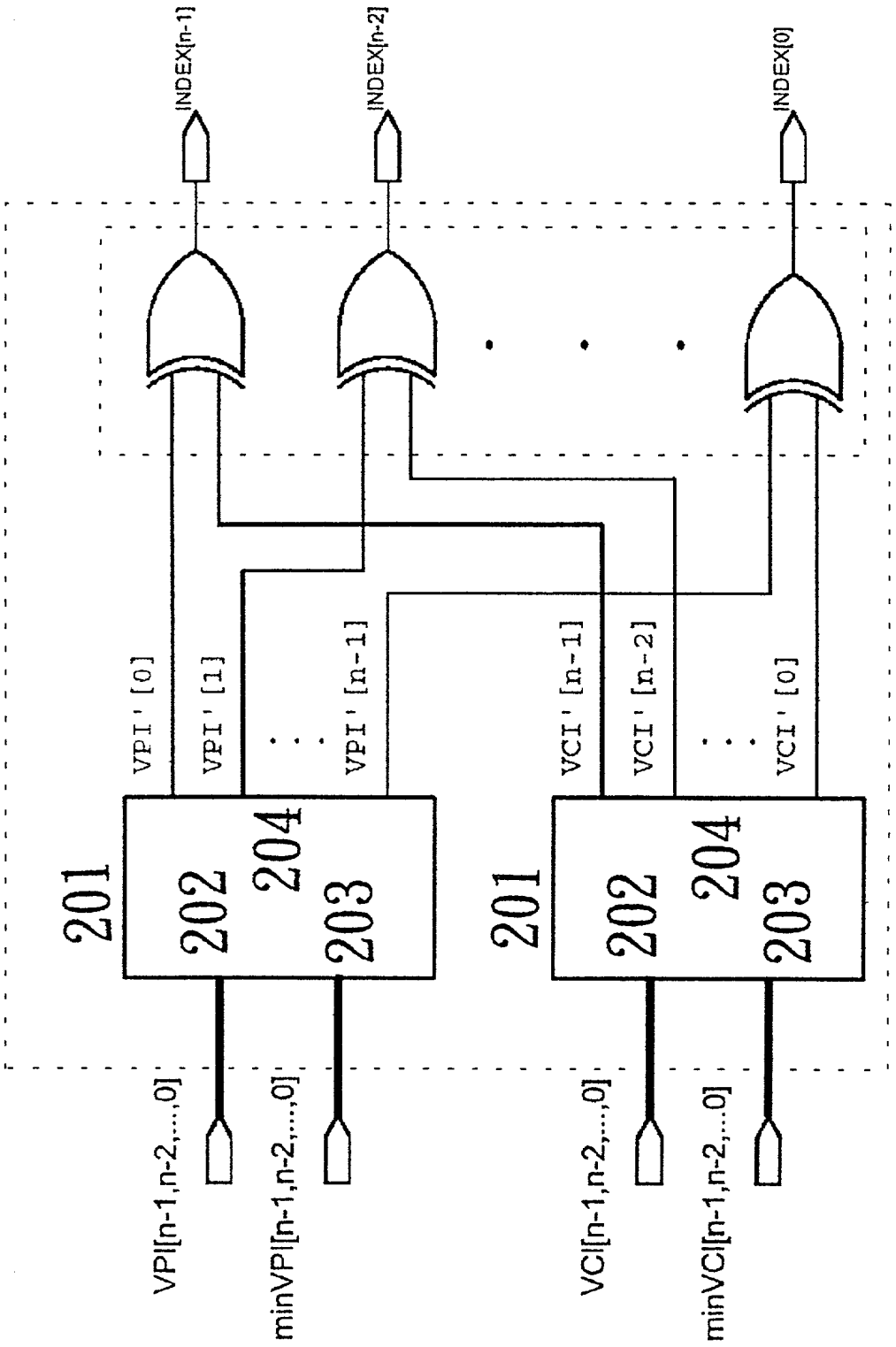
INDEX[n-1]
INDEX[n-2]
INDEX[0]
VPI'[0]
VPI'[1]
VPI'[n-1]
VCI'[n-1]
VCI'[n-2]
VCI'[0]
201
202
204
203
201
202
204
203
VPI[n-1,n-2,...,0]
minVPI[n-1,n-2,...,0]
VCI[n-1,n-2,...,0]
minVCI[n-1,n-2,...0]

FIG 2

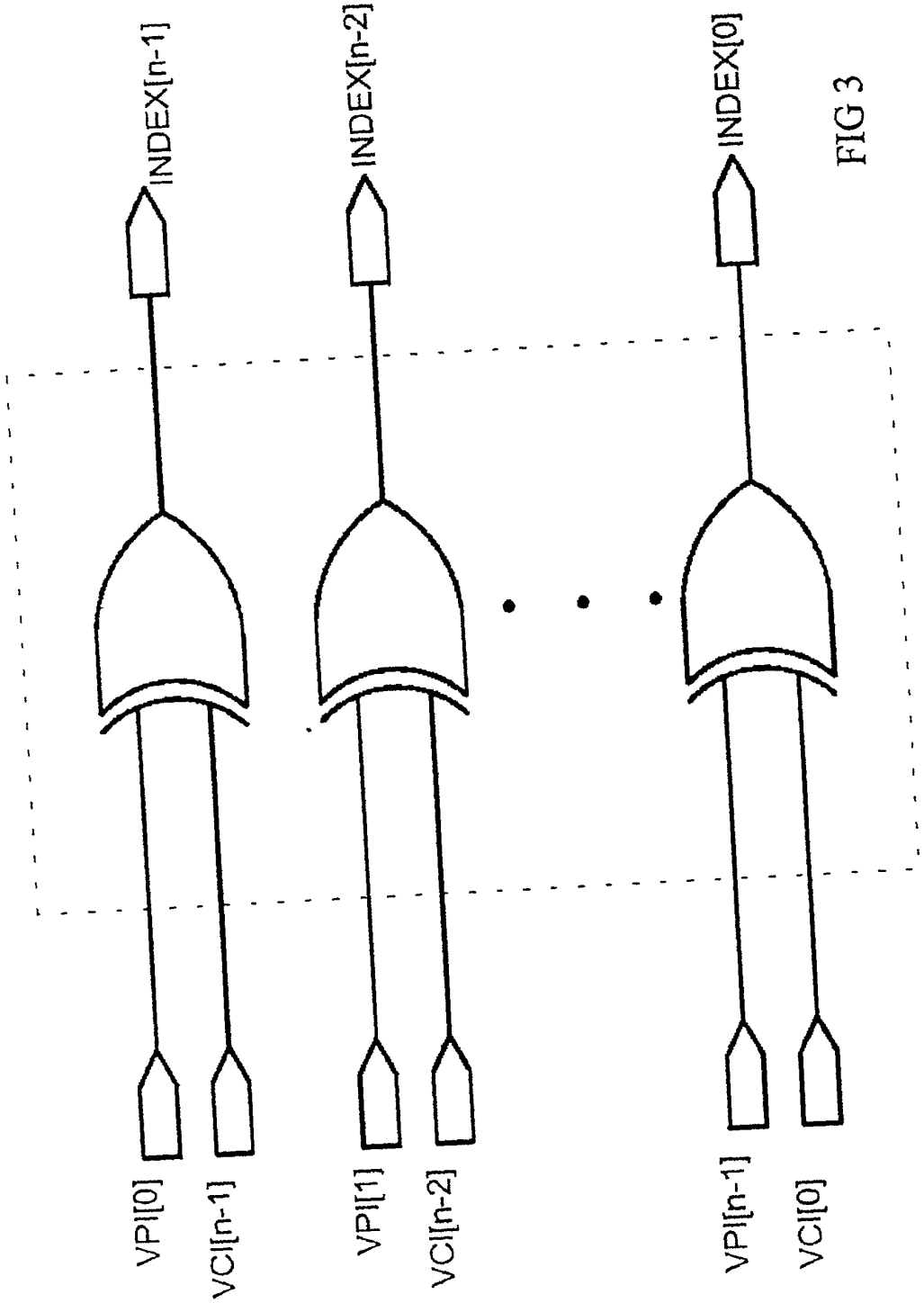

FIG 3

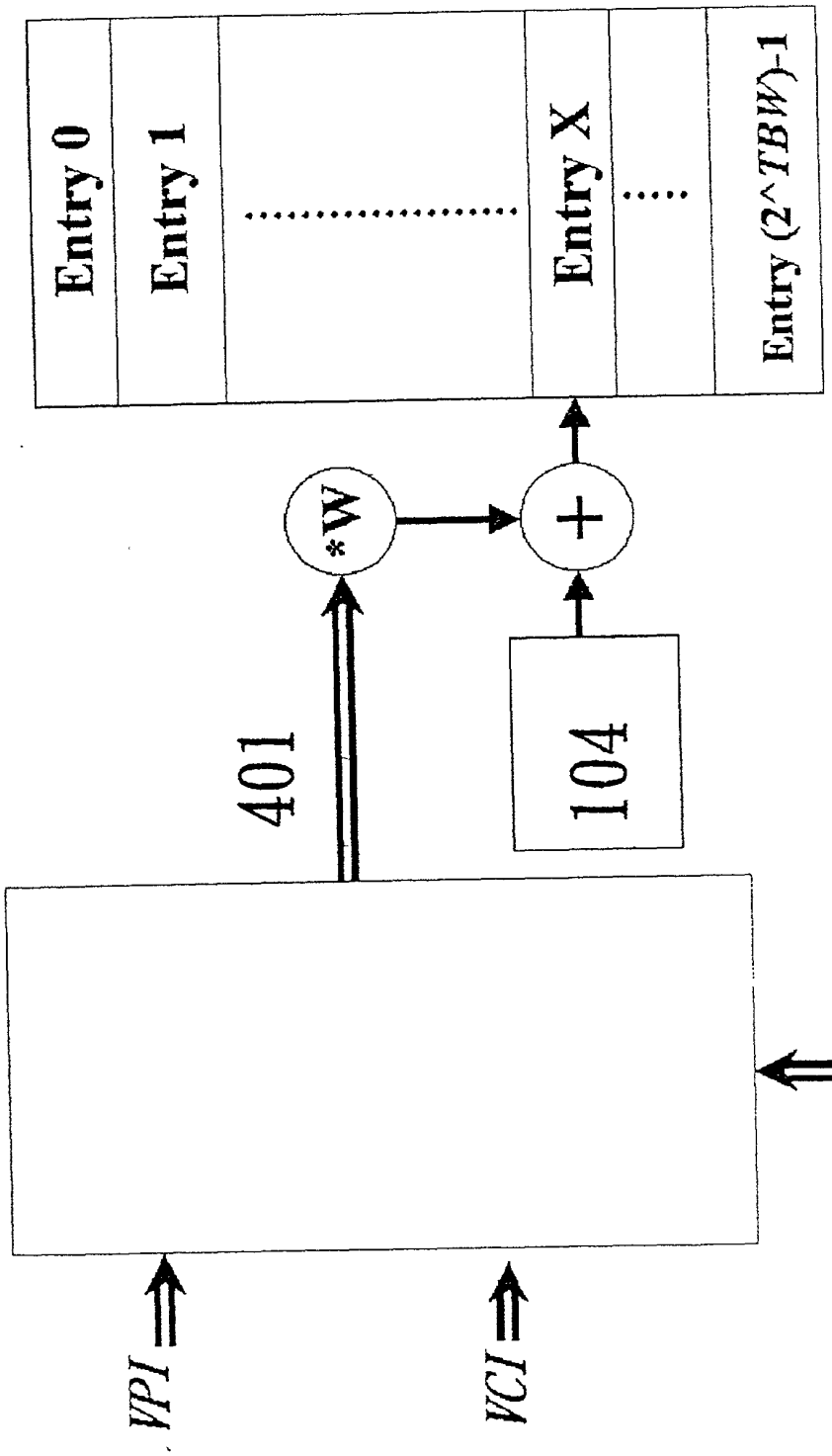

FIG 4

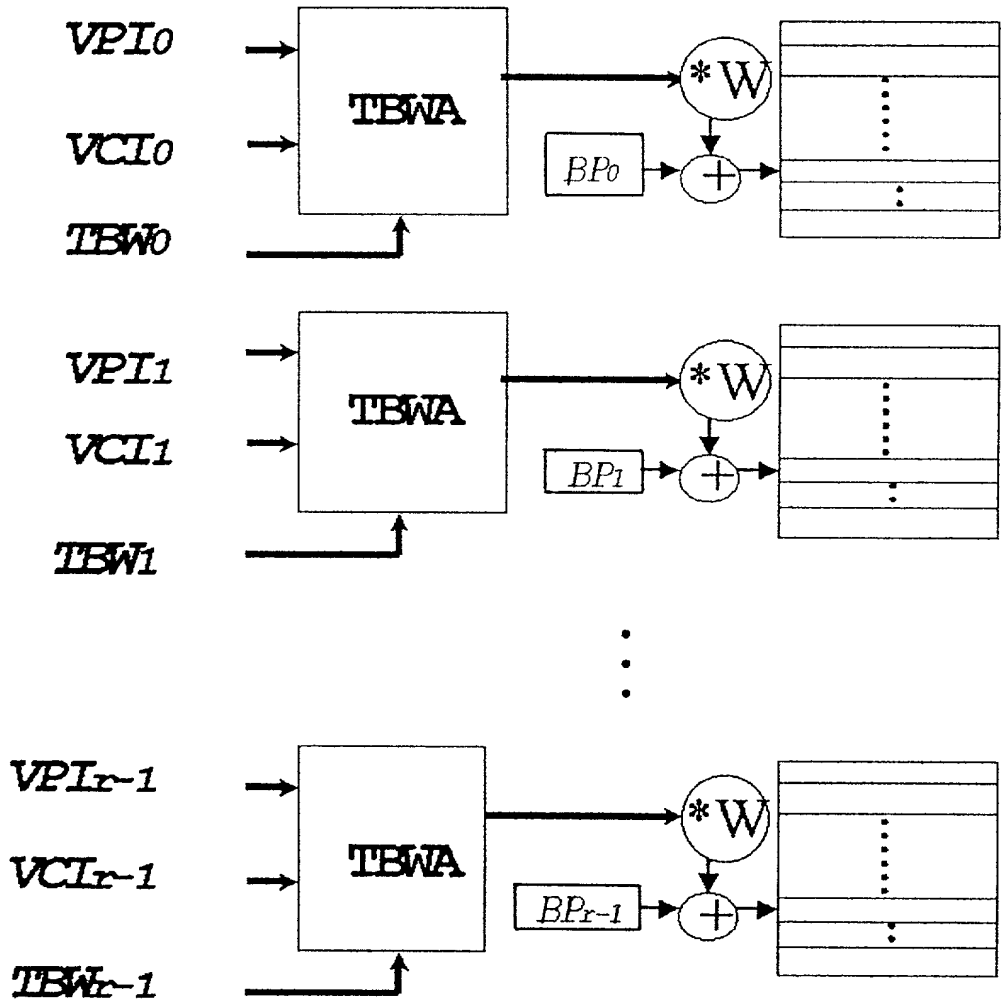
VPI0
VCI0
TBW0
TBWA
*W
BP0
VPI1
VCI1
TBW1
TBWA
*W
BP1
VPIr-1
VCIr-1
TBWr-1
TBWA
*W
BPr-1

FIG 5

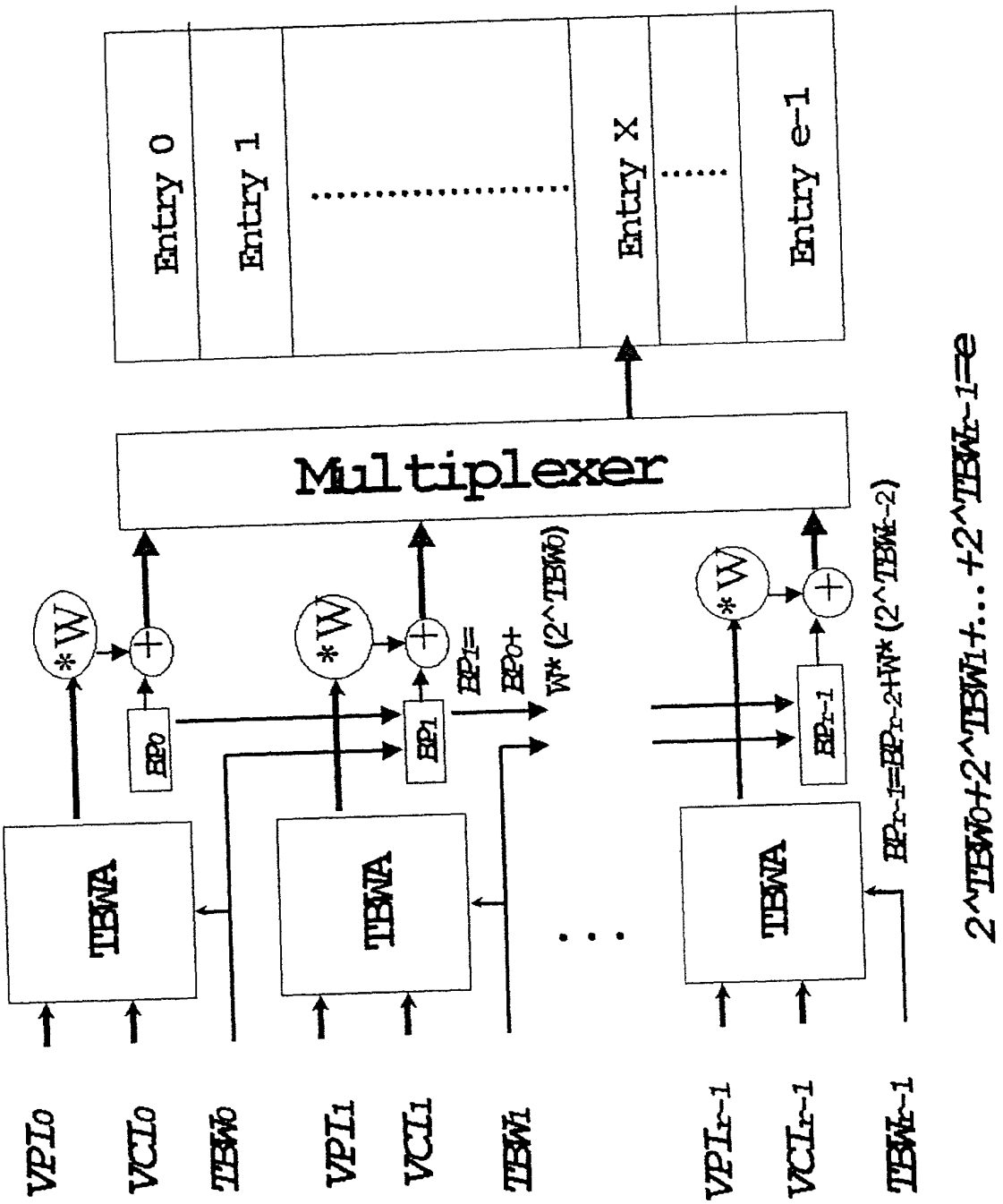
Entry 0
Entry 1
Entry X
Entry e-1
Multiplexer
*W
TBWA
VPI0
VCI0
TBW0
VPI1
VCI1
TBW1
VPIr-1
VCIr-1
TBWr-1
BP0
BP1
BPr-1
2^TBW0+2^TBW1+...+2^TBWr-1=e

FIG 6